ATmega32 Reference Guide

Ver. 1.0
9-20-2005

1 Features

High-performance, Low-power RISC Architecture 8-bit Microcontroller
- 32 x 8 General Purpose Working Registers
- Fully Static Operation, up to 16 MIPS Throughput at 16 MHz
- On-chip 2-cycle Multiplier

Nonvolatile Program and Data Memories
- 32K Bytes of In-System Self-Programmable Flash, Endurance: 10,000 Write/Erase Cycles
- Optional Boot Code Section with Independent Lock Bits
- In-System Programming by On-chip Boot Program, true Read-While-Write Operation
- 1024 Bytes EEPROM, Endurance: 100,000 Write/Erase Cycles
- 2K Byte Internal SRAM
- Programming Lock for Software Security

JTAG (IEEE std. 1149.1 Compliant) Interface, Boundary-scan Capabilities
- Extensive On-chip Debug Support, Programming of Flash, EEPROM, Fuses, and Lock Bits

Peripheral Features
- Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
- One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
- Real Time Counter with Separate Oscillator
- Four PWM Channels
- 8-channel, 10-bit ADC
  - 8 Single-ended Channels, 7 Differential Channels in TQFP Package Only
  - 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
- Byte-oriented Two-wire Serial Interface
- Programmable Serial USART
- Master/Slave SPI Serial Interface
- Programmable Watchdog Timer with Separate On-chip Oscillator
- On-chip Analog Comparator

Special Microcontroller Features
- Power-on Reset and Programmable Brown-out Detection
- Internal Calibrated RC Oscillator
- External and Internal Interrupt Sources
- Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby

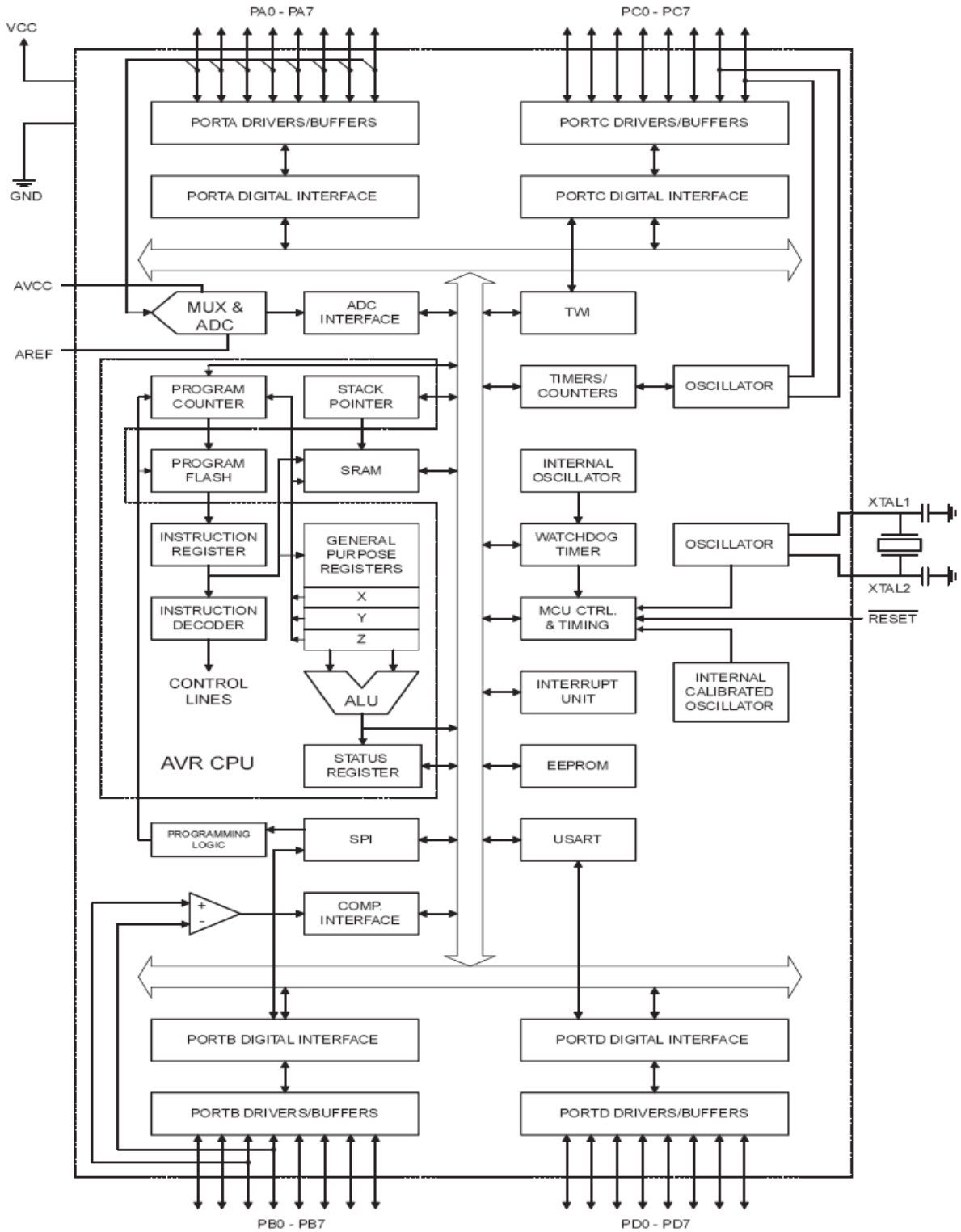
I/O and Packages
- 32 Programmable I/O Lines
- 40-pin PDIP, 44-lead TQFP, and 44-pad MLF

Operating Voltages
- 2.7 - 5.5V for ATmega32L
- 4.5 - 5.5V for ATmega32

Speed Grades
- 0 - 8 MHz for ATmega32L, 0 - 16 MHz for ATmega32

Power Consumption at 1 MHz, 3V, 25×C for ATmega32L
- Active: 1.1 mA
- Idle Mode: 0.35 mA
- Power-down Mode:< 1 ìA

2 Block Diagram



3 Programming Model

7 … 0	Addr.	
R0	$00	
R1	$01	
R2	$02	
R3	$03	
...		
R12	$0C	
R13	$0D	
R14	$0E	
R15	$0F	
R16	$10	
R17	$11	
...		
R26	$1A	X-register Low Byte
R27	$1B	X-register High Byte
R28	$1C	Y-register Low Byte
R29	$1D	Y-register High Byte
R30	$1E	Z-register Low Byte
R31	$1F	Z-register High Byte

	15	XH	0	7	XL	0
X-register	7	R27	0	7	R26	0
Y-register	7	R29	0	7	R28	0
Z-register	7	R31	0	7	R30	0

Bit	7	6	5	4	3	2	1	0
	I	T	H	S	V	N	Z	C
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

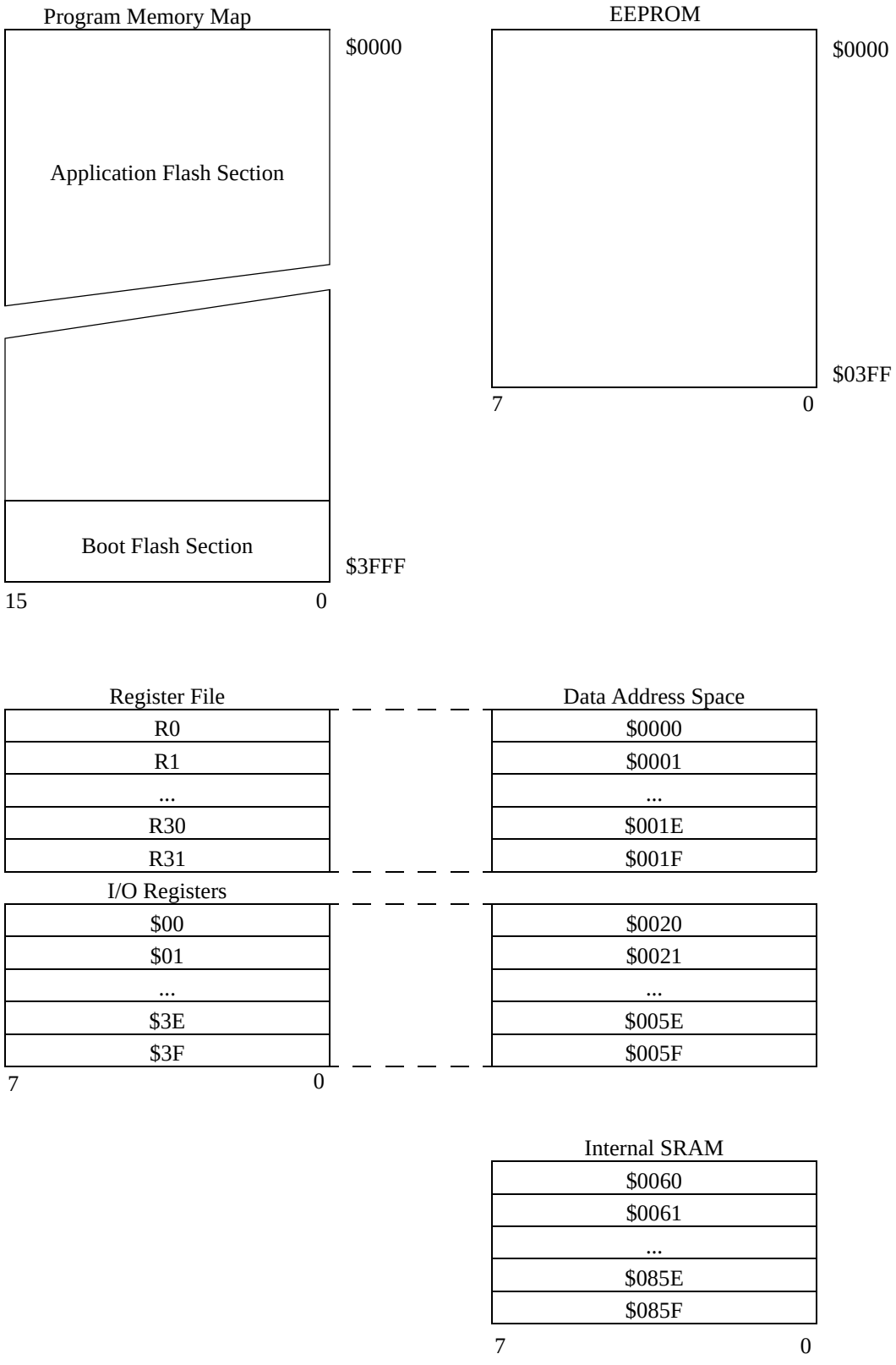
I - Global Interrupt Enable
C - carry flag
N - Negative Flag
S - Sign Bit, S = N EXOR V
T - Bit Copy Storage
Z - Zero Flag
V - Two’s Complement Overflow Flag
H - Half Carry Flag

4 Interrupt Vector Assignments

Vector No.	Program Address	Source	Interrupt
1	$0000	RESET	External Pin, Power-on Reset, Brown-out Reset, Watchdog Reset, and JTAG AVR Reset
2	$0002	INT0	External Interrupt Request 0
3	$0004	INT1	External Interrupt Request 1
4	$0006	INT2	External Interrupt Request 2
5	$0008	TIMER2 COMP	Timer/Counter2 Compare Match
6	$000A	TIMER2 OVF	Timer/Counter2 Overflow
7	$000C	TIMER1 CAPT	Timer/Counter1 Capture Event
8	$000E	TIMER1 COMPA	Timer/Counter1 Compare Match A
9	$0010	TIMER1 COMPB	Timer/Counter1 Compare Match B
10	$0012	TIMER1 OVF	Timer/Counter1 Overflow
11	$0014	TIMER0 COMP	Timer/Counter0 Compare Match
12	$0016	TIMER0 OVF	Timer/Counter0 Overflow
13	$0018	SPI STC	Serial Transfer Complete
14	$001A	USART RXC	USART, Rx Complete
15	$001C	USART UDRE	USART Data Register Empty
16	$001E	USART TXC	USART, Tx Complete
17	$0020	ADC	ADC Conversion Complete
18	$0022	EE_RDY	EEPROM Ready
19	$0024	ANA_COMP	Analog Comparator
20	$0026	TWI	Two-wire Serial Interface
21	$0028	SPM_RDY	Store Program Memory Ready

- When the BOOTRST fuse is programmed, the device will jump to the Boot Loader address at reset.
- When the IVSEL bit in GICR is set, interrupt vectors will be moved to the start of the Boot Flash section. The address of each Interrupt Vector will then be the address in this table added to the start address of the Boot Flash section.

5 Memory Maps



5.1 Instruction Set

Mnemonic	Ops.	Description	Operation	Flags	Cyc.
Arithmetic and Logic Instructions					
ADD	Rd,Rr	Add without carry	Rd=Rd+Rr	Z,C,N,V,H,S	1
ADC	Rd,Rr	Add with carry	Rd=Rd+Rr+C	Z,C,N,V,H,S	1
ADIW	Rd,K	Add immediate to word	Rd+1:Rd=Rd+1:Rd+K6 d=24,26,28,30	Z,C,N,V,S	2
SUB	Rd,Rr	Subtract without carry	Rd=Rd-Rr	Z,C,N,V,H,S	1
SUBI	Rd,Rr	Subtract immediate	Rd=Rd-K8 d=16...31	Z,C,N,V,H,S	1
SBC	Rd,Rr	Subtract with carry	Rd=Rd-Rr-C	Z,C,N,V,H,S	1
SBCI	Rd,K8	Subtract with carry immediate	Rd-Rd-K8-C d=16...31	Z,C,N,V,H,S	1
SBIW	Rd,K	Subtract Immediate from Word	Rd+1:Rd=Rd+1:Rd-K6 d=24,26,28,30		
AND	Rd,Rr	Logical AND	Rd=Rd AND Rr	Z,N,V,S	1
ANDI	Rd,K8	Logical AND with immediate	Rd=Rd AND k8 d=16...31	Z,N,V,S	1
OR	Rd,Rr	Logical OR	Rd=Rd OR Rr	Z,N,V,S	1
ORI	Rd,K8	Logical OR with immediate	Rd=Rd OR K8 d=16...31	Z,N,V,S	1
EOR	Rd,Rr	Logical EXOR	Rd=Rd EXOR Rr	Z,N,V,S	1
COM	Rd	One’s complement	Rd=$FF-Rd	Z,C,N,V,S	1
NEG	Rd	Two’s complement	Rd=$00-Rd	Z,C,N,V,H,S	1
SBR	Rd,K8	Set bit(s) in register	Rd=Rd OR K8	Z,C,N,V,S	1
CBR	Rd,k8	Clear bit(s) in register	Rd=Rd*($FF-k8) d=16...31	Z,C,N,V,S	1
INC	Rd	Increment register	Rd=Rd+1	Z,N,V,S	1
DEC	Rd	Decrement register	Rd=Rd-1	Z,N,V,S	1
TST	Rd	Test for zero or negative	Rd=Rd AND RD	Z,C,N,V,S	1
CLR	Rd	Clear register	Rd=0	Z,C,N,V,S	1
SER	Rd	Set register	Rd=$FF d=16...31	None	1
SBIW	Rd,K6	Subtract immediate from word	Rd+1:Rd=Rd+1:Rd-k6	Z,C,N,V,S	2
MUL	Rd,Rd	Multiply unsigned	R1:R0=Rd*Rr	Z,C	2
MULS	Rd,Rr	Multiply signed	R1:R0=Rd*Rr	Z,C	2
MULSU	Rd,Rr	Multiply signed with unsigned	R1:R0=Rd*Rr	Z,C	2
FMUL	Rd,Rr	Fractional multiply unsigned	R1:R0=(Rd*Rr)<<1	Z,C	2
FMULS	Rd,Rr	Fractional multiply signed	R1:R0=(Rd*Rr)<<1	Z,C	2
FMULSU	Rd,Rr	Fractional multiply signed with unsigned	R1:R0=(Rd*Rr)<<1	Z,C	2

Mnemonic	Ops.	Description	Operation	Flags	Cyc.
Branch Instructions					
RJMP	K	Relative Jump	PC=PC+K+1 k= -2k...2k	None	2
IJMP	None	Indirect Jump to (Z)	PC=Z	None	2
EIJMP	None	Extended Indirect Jump to (Z)	Stack=PC+1, PC(15:0)=Z, PC(21:16)=EIND	None	2
JMP	K	Jump	PC=K	None	3
RCALL	K	Relative Call Subroutine	Stack=PC+1, PC=PC+K+1 k= -2k...2k	None	3/4
ICALL	None	Indirect Call to (Z)	Stack=PC+1, PC=(Z)	None	3/4
CALL	K	Call Subroutine	Stack=PC+2, PC=K	None	4/5
RET	None	Subroutine Return	PC=Stack	None	4/5
RETI	None	Interrupt Return	PC=Stack	I	4/5
CPSE	Rd,Rr	Compare, Skip if Equal	if(Rd==Rr) PC=PC+2/3	None	1/2/3
CP	Rd,Rr	Compare	Rd-Rr	Z,C,N,V,H,S	1
CPC	Rd,Rr	Compare with Carry	Rd-Rr-C	Z,C,N,V,H,S	1
CPI	Rd,K8	Compare with Immediate	Rd-K8 d=16...31	Z,C,N,V,H,S	1
SBRC	Rr,b	Skip if bit in register cleared	if(Rr(b)==0) PC=PC+2/3 b=0...7	None	1/2/3
SBRS	Rr,b	Skip if bit in register set	if(Rr(b)==1) PC=PC+2/3 b=0...7	None	1/2/3
SBIC	P,b	Skip if bit in I/O register cleared	if(I/O(P,b)==0) PC=PC+2/3 b=0...7	None	1/2/3
SBIS	P,b	Skip if bit in I/O register set	if(I/O(P,b)==1) PC=PC+2/3 b=0...7	None	1/2/3
BRBC	s,k	Branch if Status flag cleared	if(SREG(s)==0) PC = PC + k + 1 k= -64...63	None	1/2
BRBS	s,k	Branch if Status flag set	if(SREG(s)==1) PC = PC + k + 1 k= -64...63	None	1/2
BREQ	k	Branch if equal	if(Z==1) PC = PC + k + 1 k= -64...63	None	1/2
BRNE	k	Branch if not equal	if(Z==0) PC = PC + k + 1 k= -64...63	None	1/2
BRCS	k	Branch if carry set	if(C==1) PC = PC + k + 1 k= -64...63	None	1/2
BRCC	k	Branch if carry cleared	if(C==0) PC = PC + k + 1 k= -64...63	None	1/2
BRSH	k	Branch if same or higher	if(C==0) PC = PC + k + 1 k= -64...63	None	1/2
BRLO	k	Branch if lower	if(C==1) PC = PC + k + 1 k= -64...63	None	1/2
BRMI	k	Branch if minus	if(N==1) PC = PC + k + 1 k= -64...63	None	1/2
BRPL	k	Branch if plus	if(N==0) PC = PC + k + 1 k= -64...63	None	1/2
BRGE	k	Branch if greater than or equal (signed)	if(S==0) PC = PC + k + 1 k= -64...63	None	1/2
BRLT	k	Branch if less than (signed)	if(S==1) PC = PC + k + 1 k= -64...63	None	1/2
BRHS	k	Branch if half carry flag set	if(H==1) PC = PC + k + 1 k= -64...63	None	1/2
BRHC	k	Branch if half carry flag set	if(H==1) PC = PC + k + 1 k= -64...63	None	1/2
BRTS	k	Branch if T flag set	if(T==1) PC = PC + k + 1 k= -64...63	None	1/2
BRTC	k	Branch if T flag cleared	if(T==0) PC = PC + k + 1 k= -64...63	None	1/2
BRVS	k	Branch if overflow flag set	if(V==1) PC = PC + k + 1 k= -64...63	None	1/2
BRVC	k	Branch if overflow flag cleared	if(V==0) PC = PC + k + 1 k= -64...63	None	1/2
BRIE	k	Branch if interrupt enabled	if(I==1) PC = PC + k + 1 k= -64...63	None	1/2
BRID	k	Branch if interrupt disabled	if(I==0) PC = PC + k + 1 k= -64...63	None	1/2

Mnemonic	Operands	Description	Operation	Flags	Cyc.
Data Transfer Instructions					
MOV	Rd,Rr	Copy register	Rd=Rr	None	1
MOVW	Rd,Rr	Copy register pair	Rd+1:Rd=Rr+1:Rr, r,d even	None	1
LDI	Rd,K8	Load immediate	Rd=K d=16...31	None	1
LDS	Rd,K	Load Direct	Rd=(K)	None	2
LD	Rd,X	Load Indirect	Rd = (X)	None	2
LD	Rd,X+	Load Indirect and Post-Increment	Rd = (X), X=X+1	None	2
LD	Rd,-X	Load Indirect and Pre-Decrement	X=X-1, Rd = (X)	None	2
LD	Rd,Y	Load Indirect	Rd = (Y)	None	2
LD	Rd,Y+	Load Indirect and Post-Increment	Rd = (Y), Y=Y+1	None	2
LD	Rd,-Y	Load Indirect and Pre-Decrement	Y=Y-1, Rd = (Y)	None	2
LDD	Rd,Y+q	Load Indirect with displacement	Rd = (Y+q)	None	2
LD	Rd,Z	Load Indirect	Rd = (Z)	None	2
LD	Rd,Z+	Load Indirect and Post-Increment	Rd = (Z), Z=Z+1	None	2
LD	Rd,-Z	Load Indirect and Pre-Decrement	Z=Z-1, Rd = (Z)	None	2
LDD	Rd,Z+q	Load Indirect with displacement	Rd = (Z+q)	None	2
STS	k,Rr	Store Direct	(k) = Rr	None	2
ST	X,Rr	Store Indirect	(X) = Rr	None	2
ST	X+,Rr	Store Indirect and Post-Increment	(X) = Rr, X=X+1	None	2
ST	-X,Rr	Store Indirect and Pre-Decrement	X=X-1, (X)=Rr	None	2
ST	Y,Rr	Store Indirect	(Y) = Rr	None	2
ST	Y+,Rr	Store Indirect and Post-Increment	(Y) = Rr, Y=Y+1	None	2
ST	-Y,Rr	Store Indirect and Pre-Decrement	Y=Y-1, (Y) = Rr	None	2
ST	Y+q,Rr	Store Indirect with displacement	(Y+q) = Rr	None	2
ST	Z,Rr	Store Indirect	(Z) = Rr	None	2
ST	Z+,Rr	Store Indirect and Post-Increment	(Z) = Rr, Z=Z+1	None	2
ST	-Z,Rr	Store Indirect and Pre-Decrement	Z=Z-1, (Z) = Rr	None	2
ST	Z+q,Rr	Store Indirect with displacement	(Z+q) = Rr	None	2
LPM	None	Load Program Memory	R0 = (Z)	None	3
LPM	Rd,Z	Load Program Memory	Rd = (Z)	None	3
LPM	Rd,Z+	Load Program Memory and Post-Increment	Rd = (Z), Z=Z+1	None	3
SPM	None	Store Program Memory	(Z) = R1:R0	None	-
IN	Rd,P	In Port	Rd = P	None	1
OUT	P,Rr	Out Port	P = Rr	None	1

Mnemonic	Operands	Description	Operation	Flags	Cyc.
Bit and Bit-Test Instruction					
LSL	Rd	Logical shift left	Rd(n+1)=Rd(n), Rd(0)=0, C=Rd(7)	Z,C,N,V,H,S	1
LSR	Rd	Logical shift right	Rd(n)=Rd(n+1), Rd(7)=0, C=Rd(0)	Z,C,N,V,S	1
ROL	Rd	Rotate left through carry	Rd(0)=C, Rd(n+1)=Rd(n), C=Rd(7)	Z,C,N,V,H,S	1
ROR	Rd	Rotate right through carry	Rd(7)=C, Rd(n)=Rd(n+1), C=Rd(0)	Z,C,N,V,S	1

Mnemonic	Operands	Description	Operation	Flags	Cyc.
ASR	Rd	Arithmetic shift right	Rd(n)=Rd(n+1), n=0,...,6	Z,C,N,V,S	1
SWAP	Rd	Swap nibbles	Rd(3..0) = Rd(7..4), Rd(7..4) = Rd(3..0)	None	1
BSET	s	Set flag	SREG(s) = 1	SREG(s)	1
BCLR	s	Clear flag	SREG(s) = 0	SREG(s)	1
SBI	P,b	Set bit in I/O register	I/O(P,b) = 1 P=0...31 b =0...7	None	2
CBI	P,b	Clear bit in I/O register	I/O(P,b) = 0 P=0...31 b=0...7	None	2
BST	Rr,b	Bit store from register to T	T = Rr(b)	T	1
BLD	Rd,b	Bit load from register to T	Rd(b) = T	None	1
SEC	None	Set carry flag	C =1	C	1
CLC	None	Clear carry flag	C = 0	C	1
SEN	None	Set negative flag	N = 1	N	1
CLN	None	Clear negative flag	N = 0	N	1
SEZ	None	Set zero flag	Z = 1	Z	1
CLZ	None	Clear zero flag	Z = 0	Z	1
SEI	None	Set interrupt flag	I = 1	I	1
CLI	None	Clear interrupt flag	I = 0	I	1
SES	None	Set signed flag	S = 1	S	1
CLN	None	Clear signed flag	S = 0	S	1
SEV	None	Set overflow flag	V = 1	V	1
CLV	None	Clear overflow flag	V = 0	V	1
SET	None	Set T-flag	T = 1	T	1
CLT	None	Clear T-flag	T = 0	T	1
SEH	None	Set half carry flag	H = 1	H	1
CLH	None	Clear half carry flag	H = 0	H	1
NOP	None	No operation	None	None	1
SLEEP	None	Sleep	See instruction manual	None	1
WDR	None	Watchdog Reset	See instruction manual	None	1
BREAK	None	Execution Break	See instruction manual	None	1

Rd: Destination (and source) register in the register file
Rr: Source register in the register file
b: Constant (0-7), can be a constant expression
s: Constant (0-7), can be a constant expression
P: Constant (0-31/63), can be a constant expression
K6; Constant (0-63), can be a constant expression
K8: Constant (0-255), can be a constant expression
k: Constant, value range depending on instruction. Can be a constant expression
q: Constant (0-63), can be a constant expression
Rdl: R24, R26, R28, R30. For ADIW and SBIW instructions
X,Y,Z: Indirect address registers (X=R27:R26, Y=R29:R28, Z=R31:R30)

6 Register Summary

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$3F($5F)	SREG	I	T	H	S	V	N	Z	C
$3E($5E)	SPH	–	–	–	–	SP11	SP10	SP9	SP8
$3D($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
$3C($5C)	OCR0	Timer/Counter0 Output Compare Register							
$3B($5B)	GICR	INT1	INT0	INT2	–	–	–	IVSEL	IVCE
$3A($5A)	GIFR	INTF1	INTF0	INTF2	–	–	–	–	–
$39($59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0
$38($58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0
$37($57)	SPMCR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN
$36($56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE
$35($55)	MCUCR	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00
$34($54)	MCUCSR	JTD	ISC2	–	JTRF	WDRF	BORF	EXTRF	PORF
$33($53)	TCCR0	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00
$32($52)	TCNT0	Timer/Counter0 (8 Bits)							
$31($51)	OSCCAL	Oscillator Calibration Register							
	OCDR	On-Chip Debug Register							
$30($50)	SFIOR	ADTS2	ADTS1	ADTS0	–	ACME	PUD	PSR2	PSR10
$2F($4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10
$2E($4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10
$2D($4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte							
$2C($4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte							
$2B($4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High Byte							
$2A($4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low Byte							
$29($49)	OCR1BH	Timer/Counter1 – Output Compare Register B High Byte							
$28($48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low Byte							
$27($47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte							
$26($46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte							
$25($45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20
$24($44)	TCNT2	Timer/Counter2 (8 Bits)							
$23($43)	OCR2	Timer/Counter2 Output Compare Register							
$22($42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB
$21($41)	WDTCR	–	–	–	WDTOE	WDE	WDP2	WDP1	WDP0
$20($40)	UBRRH	URSEL	–	–	–	UBRR[11:8]			
UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	160
$1F($3F)	EEARH	–	–	–	–	–	–	EEAR9	EEAR8
$1E($3E)	EEARL	EEPROM Address Register Low Byte							
$1D($3D)	EEDR	EEPROM Data Register							
$1C($3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE
$1B($3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0
$1A($3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
$19($39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0
$18($38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0
$17($37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$16($36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0
$15($35)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0
$14($34)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
$13($33)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0
$12($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0
$11($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
$10($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0
$0F($2F)	SPDR	SPI Data Register							
$0E($2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X
$0D($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
$0C($2C)	UDR	USART I/O Data Register							
$0B($2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM
$0A($2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8
$09($29)	UBRRL	USART Baud Rate Register Low Byte							
$08($28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0
$07($27)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0
$06($26)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
$05($25)	ADCH	ADC Data Register High Byte							
$04($24)	ADCL	ADC Data Register Low Byte							
$03($23)	TWDR	Two-wire Serial Interface Data Register							
$02($22)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE

7 Registers

7.1 Core

Status Register - SREG

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- I - Global Interrupt Enable
  0 : disable
  1 : enable
- T - Bit Copy Storage
- C - carry flag
- Z - Zero Flag
- N - Negative Flag
- V - Two’s Complement Overflow Flag
- S - Sign Bit, S = N EXOR V
- H - Half Carry Flag
- T - bit copy storage

Stack Pointer - SPH, SPL

Bit	15	14	13	12	11	10	9	8	
	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SPH
	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

7.2 EEPROM

EEPROM Address Register - EEARH, EEARL

Bit	15	14	13	12	11	10	9	8	
	-	-	-	-	-	-	EEAR9	EEAR8	EEARH
	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	EEARL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	x	x	
	x	x	x	x	x	x	x	x	

EEPROM Data Register - EEDR

Bit	7	6	5	4	3	2	1	0	
	MSB							LSB	EEDR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

EEPROM Control Register - EECR

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	EERIE	EEMWE	EEWE	EERE	EECR
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	x	0	

- EERIE - EEPROM Ready Interrupt Enable
  0 : disable
  1 : enable

- EEMWE - EEPROM Master Write Enable
  When EEMWE is set, setting EEWE within four clock cycles will write data to the EEPROM at the selected address.
  If EEMWE is zero, setting EEWE will have no effect.

- EEWE - EEPROM Write Enable
  EEWE is the write strobe to the EEPROM.
  1. Wait until EEWE becomes zero.
  2. Wait until SPMEN in SPMCR becomes zero.
  3. Write new EEPROM address to EEAR (optional).
  4. Write new EEPROM data to EEDR (optional).
  5. Write a logical one to the EEMWE bit while writing a zero to EEWE in EECR.
  6. Within four clock cycles after setting EEMWE, write a logical one to EEWE.

  Typ. EEPROM Programming Times : 8.5ms

- EERE - EEPROM Read Enable

EERE – is the read strobe to the EEPROM.
When the correct address is set up in the EEAR Register, the EERE bit must be written to a logic one to trigger the EEPROM read. The EEPROM read access takes one instruction, and the requested data is available immediately. When the EEPROM is read, the CPU is halted for four cycles before the next instruction is executed.

7.3 System Clock and Clock Options

Oscillator Calibration Register - OSCCAL

Bit	7	6	5	4	3	2	1	0	
	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	OSCCAL
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	Device Specific Calibration Value								

7.4 Power Management and Sleep Modes

MCU Control Register - MCUCR

Bit	7	6	5	4	3	2	1	0	
	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- SE - Sleep Enable
  0 : disable
  1 : enable

- SM2...0 - Sleep Mode Select Bits

SM2	SM1	SM0	Sleep Mode
0	0	0	Idle
0	0	1	ADC Noise Reduction
0	1	0	Power-down
0	1	1	Power-save
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Standby (only with external oscillator)
1	1	1	Extended Standby (only with external oscillator)

7.5 System Control and Reset

MCU Control and Status Register - MCUCSR

Bit	7	6	5	4	3	2	1	0	
	JTD	ISC2	-	JTRF	WDRF	BORF	EXTRF	PORF	MCUCSR
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	See Bit Description					

- JTRF - JTAG Reset Flag
- WDRF - Watchdog Reset Flag
- BORF- Brown-out Reset Flag
- EXTRF - External Reset Flag
- PORF - Power-on Reset Flag

Watchdog Timer Control Register - WDTCR

Bit	7	6	5	4	3	2	1	0	
	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	WDTCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- WDTOE - Watchdog Turn-off Enable
  This bit must be set when the WDE bit is written to logic zero. Hardware will clear this bit after four clock cycles.

- WDE - Watchdog Enable
  0 : disable
  1 : enable
  WDE can only be cleared if the WDTOE bit has logic level one.
  To disable an enabled Watchdog Timer, the following procedure must be followed:
  1. In the same operation, write a logic one to WDTOE and WDE.
     A logic one must be written to WDE even though it is set to one before the disable operation starts.
  2. Within the next four clock cycles, write a logic 0 to WDE. This disables the Watchdog.

- WP2...WDP0 - Watchdog Timer Prescaler 2...0

WDP 2	WDP 1	WDP 0	Number of WDT Oscillator Cycles	Typical Time-out for Vcc=3.0V	Typical Time-out for Vcc=5V
0	0	0	16384	17.1ms	16.3ms
0	0	1	32768	34.3ms	32.5ms
0	1	0	65536	68.5ms	65ms
0	1	1	131072	0.14s	0.13s

WDP 2	WDP 1	WDP 0	Number of WDT Oscillator Cycles	Typical Time-out for Vcc=3.0V	Typical Time-out for Vcc=5V
1	0	0	262144	0.27s	0.26s
1	0	1	524288	0.55s	0.52s
1	1	0	1048576	1.1s	1.0s
1	1	1	2097152	2.2s	2.1s

7.6 Interrupts

General Interrupt Control Register - GICR

Bit	7	6	5	4	3	2	1	0	
	INT1	INT0	INT2	-	-	-	IVSEL	IVCE	GICR
Read/Write	R/W	R/W	R/W	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- IVSEL - Interrupt Vector Select
  0 : Interrupt vectors are placed at the start of Flash memory
  1 : Interrupt vectors are placed at the start of the Boot Loader section
  To avoid unintentional changes of Interrupt Vector tables, a special write procedure must be followed to change the IVSEL bit:
  1. Write the Interrupt Vector Change Enable (IVCE) bit to one.
  2. Within four cycles, write the desired value to IVSEL while writing a zero to IVCE.

- IVCE - Interrupt Vector Change Enable
  The IVCE bit must be written to logic one to enable change of the IVSEL bit. IVCE is cleared by hardware four cycles after it is written or when IVSEL is written. Setting the IVCE bit will disable interrupts.

7.7 I/O Ports

Special Function I/O Register - SFIOR

Bit	7	6	5	4	3	2	1	0	
	ADTS2	ADTS1	ADTS0	-	ACME	PUD	PSR2	PSR10	SFIOR
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- PUD - Pull-up disable
  0 : Pull-up resistors connected
  1 : Pull-up resistors disconnected

Port A Data Register - PORTA

Bit	7	6	5	4	3	2	1	0	
	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	PORTA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port A Data Direction Register - DDRA

Bit	7	6	5	4	3	2	1	0	
	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port A Input Pins Address - PINA

Bit	7	6	5	4	3	2	1	0	
	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	PINA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port B Data Register - PORTB

Bit	7	6	5	4	3	2	1	0	
	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port B Data Direction Register - DDRB

Bit	7	6	5	4	3	2	1	0	
	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port B Input Pins Address - PINB

Bit	7	6	5	4	3	2	1	0	
	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port C Data Register - PORTC

Bit	7	6	5	4	3	2	1	0	
	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	PORTC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port C Data Direction Register - DDRC

Bit	7	6	5	4	3	2	1	0	
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port C Input Pins Address - PINC

Bit	7	6	5	4	3	2	1	0	
	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	PINC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port D Data Register - PORTD

Bit	7	6	5	4	3	2	1	0	
	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	PORTD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port D Data Direction Register - DDRD

Bit	7	6	5	4	3	2	1	0	
	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port D Input Pins Address - PIND

Bit	7	6	5	4	3	2	1	0	
	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	PIND
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

DDxn	PORTxn	PUD (in SFIOR)	I/O	Pull-up	Comment
0	0	x	Input	No	Tri-state (Hi-Z)
0	1	0	Input	Yes	Pxn will source current if ext. pulled low.
0	1	1	Input	No	Tri-state (Hi-Z)
1	0	x	Output	No	Output Low (Sink)
1	1	x	Output	No	Output High (Source)

7.8 External Interrupts

MCU Control Register - MCUCR

Bit	7	6	5	4	3	2	1	0	
	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- ISC11, ISC10 - Interrupt Sense Control 1

ISC11	ISC10	Description
0	0	Low level of INT1 generates interrupt request
0	1	Logical change on INT1 generates interrupt request
1	0	Falling edge of INT1 generates interrupt request
1	1	Rising edge of INT1 generates interrupt request

- ISC01, ISC00 - Interrupt Sense Control 0

ISC01	ISC00	Description
0	0	Low level of INT0 generates interrupt request
0	1	Logical change on INT0 generates interrupt request
1	0	Falling edge of INT0 generates interrupt request
1	1	Rising edge of INT0 generates interrupt request

MCU Control and Status Register - MCUCSR

Bit	7	6	5	4	3	2	1	0	
	JTD	ISC2	-	JTRF	WDRF	BORF	EXTRF	PORF	MCUCSR
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	See Bit Description					

- ISC2 - Interrupt Sense Control 2
  0 : Falling edge on INT2 generates interrupt request
  1 : Rising edge on INT2 generates interrupt request

General Interrupt Control Register - GICR

Bit	7	6	5	4	3	2	1	0	
	INT1	INT0	INT2	-	-	-	IVSEL	IVCE	GICR
Read/Write	R/W	R/W	R/W	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- INT1 - External Interrupt Request 1 Enable
  0 : disable
  1 : enable

- INT0 - External Interrupt Request 0 Enable
  0 : disable
  1 : enable

- INT2 - External Interrupt Request 2 Enable
  0 : disable
  1 : enable

General Interrupt Flag Register - GIFR

Bit	7	6	5	4	3	2	1	0	
	INTF1	INTF0	INTF2	-	-	-	-	-	GIFR
Read/Write	R/W	R/W	R/W	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- INTF1 - External Interrupt Flag 1
  1 : Interrupt Request
  Flag is cleared when the interrupt routine is executed. The flag can be cleared by writing a logical one to it.

- INTF0 - External Interrupt Flag 0
  1 : Interrupt Request
  Flag is cleared when the interrupt routine is executed. The flag can be cleared by writing a logical one to it.

- INTF2 - External Interrupt Flag 2
  1 : Interrupt Request
  Flag is cleared when the interrupt routine is executed. The flag can be cleared by writing a logical one to it.

7.9 8-bit Timer/Counter0 with PWM

Timer/Counter Control Register - TCCR0

Bit	7	6	5	4	3	2	1	0	
	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	TCCR0
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- FOC0 - Force Output Compare

  Only active when the WGM00 bit specifies a non-PWM mode. When writing a logical one to the FOC0 bit, an immediate compare match is forced on the Waveform Generation unit. The OC0 output is changed according to its COM01:0 bits setting. Note that the FOC0 bit is implemented as a strobe. Therefore it is the value present in the COM01:0 bits that determines the effect of the forced compare. A FOC0 strobe will not generate any interrupt, nor will it clear the timer in CTC mode using OCR0 as TOP.

  The FOC0 bit is always read as zero.

- WGM01:0 - Waveform Generation Mode

  These bits control the counting sequence of the counter, the source for the maximum (TOP) counter value, and what type of Waveform Generation to be used.

Mode	WGM01	WGM00	Timer/Counter Mode of Operation	TOP	Update of OCR0	TOV0 Flag Set-on
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	)CR0	Immediate	MAX
3	1	1	Fast PWM	0xFF	TOP	MAX

- COM01:0 - Compare Match Output Mode

Compare Output Mode, non-PWM mode		
COM01	COM00	Description
0	0	Normal port operation, OC0 disconnected
0	1	Toggle OC0 on compare match
1	0	Clear OC0 on compare match
1	1	Set OC0 on compare match

Compare Output Mode, fast-PWM mode		
COM01	COM00	Description
0	0	Normal port operation, OC0 disconnected
0	1	Reserved
1	0	Clear OC0 on compare match, set OC0 at TOP
1	1	Set OC0 on compare match, clear OC0 at TOP

Compare Output Mode, phase correct-PWM mode		
COM01	**COM00**	**Description**
0	0	Normal port operation, OC0 disconnected
0	1	Reserved
1	0	Clear OC0 on compare match when up-counting. Set OC0 on compare match when downloading
1	1	Set OC0 on compare match when up-counting. Clear OC0 on compare match when downcounting.

- CS2:0 - Clock Select

CS02	**CS01**	**CS00**	**Description**
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	clk
0	1	0	clk/8
0	1	1	clk/64
1	0	0	clk/256
1	0	1	clk/1024
1	1	0	External clock source on T0 pin. Clock on falling edge
1	1	1	External clock source on T0 pin. Clock on rising edge

If external pin modes are used for the Timer/Counter0, transitions on the T0 pin will clock the counter even if the pin is configured as an output.

Timer/Counter Register - TCNT0

Bit	7	6	5	4	3	2	1	0	
	TCNT0[7:0]								TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Output Compare Register - OCR0

Bit	7	6	5	4	3	2	1	0	
	OCR0[7:0]								OCR0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Timer/Counter Interrupt Mask Register - TIMSK

Bit	7	6	5	4	3	2	1	0	
	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- OCIE0 - Timer/Counter0 Output Compare Match Interrupt Enable
  0 : disable

1 : enable

- TOIE0 - Timer/Counter0 Overflow Interrupt EnABLE
  0 : disable
  1 : enable

Timer/Counter Interrupt Flag Register - TIFR

Bit	7	6	5	4	3	2	1	0	
	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	TIFR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- OCF0 - Output Compare Flag 0
  Set (one) when a compare match occurs between the Timer/Counter0 and the data in OCR0. OCF0 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, OCF0 is cleared by writing a logic one to the flag.

- TOV0 - Timer/Counter0 Overflow Flag
  Set (one) when an overflow occurs in Timer/Counter0. TOV0 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV0 is cleared by writing a logic one to the flag.

7.10 Timer/Counter0 and Timer/Counter1 Prescalers

Special Function I/O Register - SFIOR

Bit	7	6	5	4	3	2	1	0	
	ADTS2	ADTS1	ADTS0	-	ACME	PUD	PSR2	PSR10	SFIOR
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- PRS10 - Prescaler Reset Timer/Counter1 and Timer/Counter0
  When this bit is written to one, the Timer/Counter1 and Timer/Counter0 prescaler will be reset. The bit will be cleared by hardware after the operation is performed. Writing a zero to this bit will have no effect.

7.11 16-bit Timer/Counter1

Timer/Counter1 Control Register A - TCCR1A

Bit	7	6	5	4	3	2	1	0	
	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	TCCR1A
Read/Write	R/W	R/W	R/W	R/W	W	W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- COM1A1:0 - Compare Output Mode for Channel A
- COM1B1:0 - Compare Output Mode for Channel B

Compare Output Mode, non-PWM		
COM1A!/COM1B1	**COM1A0/COM1B0**	**Description**
0	0	Normal port operation, OC1A/OC1B disconnected
0	1	Toggle OC1A/OC1B on compare match
1	0	Clear OC1A/OC1B on compare match
1	1	Set OC1A/OC1B on compare match

Compare Output Mode, Fast-PWM		
COM1A!/COM1B1	**COM1A0/COM1B0**	**Description**
0	0	Normal port operation, OC1A/OC1B disconnected
0	1	WGM13:0 = 15: Toggle OC1A on Compare Match, OC1B disconnected (normal port operation). For all other WGM13:0 settings, normal port operation, OC1A/OC1B disconnected
1	0	Clear OC1A/OC1B on compare match, set OC1A/OC1B at TOP
1	1	Set OC1A/OC1B on compare match, clear OC1A/OC1B at TOP

Compare Output Mode, Phase-Correct and Frequency-Correct PWM		
COM1A!/COM1B1	**COM1A0/COM1B0**	**Description**
0	0	Normal port operation, OC1A/OC1B disconnected
0	1	WGM13:0 = 9 or 14: Toggle OC1A on Compare Match, OC1B disconnected (normal port operation). For all other WGM13:0 settings, normal port operation, OC1A/OC1B disconnected.
1	0	Clear OC1A/OC1B on compare match when up-counting. Set OC1A/OC1B on compare match when downcounting
1	1	Set OC1A/OC1B on compare match when up-counting. Clear OC1A/OC1B on compare match when downcounting

- FOC1A - Force Output Compare for Channel A

- FOC1B - Force Output Compare for Channel B

  The FOC1A/FOC1B bits are only active when the WGM13:0 bits specifies a non-PWM mode. When writing a logical one to the FOC1A/FOC1B bit, an immediate compare match is forced on the Waveform Generation unit.

- WGM11:0: Waveform Generation Mode

  Combined with the WGM13:2 bits found in the TCCR1B Register, these bits control the counting sequence of the counter, the source for maximum (TOP) counter value, and what type of waveform generation to be used.

Mode	WGM13	WGM12	WGM11	WGM10	Timer/Counter Mode of Operation	TOP	Update of OCR1x	TOV1 Flag Set
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR1A	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	TOP	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	TOP	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	TOP	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICR1	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCR1A	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCR1A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1	Immediate	MAX
13	1	1	0	1	Reserved -	-	-	
14	1	1	1	0	Fast PWM	ICR1	TOP	TOP
15	1	1	1	1	Fast PWM	OCR1A	TOP	TOP

Timer/Counter1 Control Register B - TCCR1B

Bit	7	6	5	4	3	2	1	0	
	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	TCCR1B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- ICNC1 - Input Capture Noise Canceler

  0 - not active

  1 - active

  The filter function requires four successive equal valued samples of the ICP1 pin for changing its output. The input capture is therefore delayed by four Oscillator cycles when the Noise Canceler is enabled.

- ICES1 - Input Capture Edge Select

  0 - falling edge triggers input capture

  1 - rising edge triggers input capture

- WGM13:2 - Waveform Generation Mode
  See TCCR1A Register description.

- CS12:0 - Clock Select

CS12	CS11	CS10	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	clk/1 (No prescaling)
0	1	0	clk/8 (From prescaler)
0	1	1	clk/64 (From prescaler)
1	0	0	clk/256 (From prescaler)
1	0	1	clk/256 (From prescaler)
1	1	0	External clock source on T1 pin. Clock on falling edge.
1	1	1	External clock source on T1 pin. Clock on rising edge.

Timer/Counter1 - TCNT1H and TCNT1L

Bit	15	14	13	12	11	10	9	8	
	TCNT1[15:8]								TCNT1H
	TCNT1[7:0]								TCNT1L
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

Output Compare Register 1 A - OCR1AH and OCR1AL

Bit	15	14	13	12	11	10	9	8	
	OCR1A[15:8]								OCR1AH
	OCR1A[7:0]								OCR1AL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

Output Compare Register 1 B – OCR1BH and OCR1BL

Bit	15	14	13	12	11	10	9	8	
	OCR1B[15:8]								OCR1BH
	OCR1B[7:0]								OCR1BL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

Timer/Counter Interrupt Mask Register - TIMSK

Bit	7	6	5	4	3	2	1	0	
	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- TICIE1 - Timer/Counter1 Input Capture Interrupt Enable
  0 : disable
  1 : enable

- OCIE1A - Timer/Counter1 Output Compare A Match Interrupt Enable
  0 : disable
  1 : enable

- OCIE1B - Timer/Counter1 Output Compare B Match Interrupt Enable
  0 : disable
  1 : enable

- TOIE1 - Timer/Counter1 Overflow Interrupt Enable
  0 : disable
  1 : enable

Timer/Counter Interrupt Flag Register - TIFR

Bit	7	6	5	4	3	2	1	0	
	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	TIFR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- ICF1 - Timer/Counter1 Input Capture Flag
  Set when a capture event occurs on the ICP1 pin. When the Input Capture Register (ICR1) is set by the WGM13:0 to be used as the TOP value, the ICF1 Flag is set when the counter reaches the TOP value. ICF1 is automatically cleared when the Input Capture Interrupt Vector is executed. Alternatively, ICF1 can be cleared by writing a logic one to its bit location.

- OCF1A - Timer/Counter1 Output Compare A Match Flag

Set in the timer clock cycle after the counter (TCNT1) value matches the Output Compare Register A (OCR1A). Note that a Forced Output Compare (FOC1A) strobe will not set the OCF1A Flag. OCF1A is automatically cleared when the Output Compare Match A Interrupt Vector is
executed. Alternatively, OCF1A can be cleared by writing a logic one to its bit location.

- OCF1B - Timer/Counter1 Output Compare B Match Flag
  Set in the timer clock cycle after the counter (TCNT1) value matches the Output Compare Register B (OCR1B). Note that a forced output compare (FOC1B) strobe will not set the OCF1B Flag. OCF1B is automatically cleared when the Output Compare Match B Interrupt Vector is executed. Alternatively, OCF1B can be cleared by writing a logic one to its bit location.

- TOV1 - Timer/Counter1 Overflow Flag
  The setting of this flag is dependent of the WGM13:0 bits setting. In normal and CTC modes, the TOV1 Flag is set when the timer overflows. TOV1 is automatically cleared when the Timer/Counter1 Overflow interrupt vector is executed. Alternatively, TOV1 can be cleared by writing a logic one to its bit location.

7.12 8-bit Timer/Counter2 with PWM and Asynchronous Operation

Timer/Counter Control Register – TCCR2

Bit	7	6	5	4	3	2	1	0	
	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	TCCR2
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- FOC2 - Force Output Compare

  The FOC2 bit is only active when the WGM bits specify a non-PWM mode. When writing a logical one to the FOC2 bit, an immediate compare match is forced on the waveform generation unit.

- WGM21:0 - Waveform Generation Mode

Mode	WGM21	WGM20	Timer/Counter Mode of Operation	TOP	Update of OCR2	TOV2 Flag Set on
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR2	Immediate	MAX
3	1	1	Fast PWM	0xFF	TOP	MAX

- COM21:0 - Compare Match Output Mode

Compare Output Mode, non-PWM Mode		
COM21	**COM20**	**Description**
0	0	Normal port operation, OC2 disconnected.
0	1	Toggle OC2 on compare match
1	0	Clear OC2 on compare match
1	1	Set OC2 on compare match

Compare Output Mode, Fast PWM Mode		
COM21	**COM20**	**Description**
0	0	Normal port operation, OC2 disconnected.
0	1	Reserved
1	0	Clear OC2 on compare match, set OC2 at TOP
1	1	Set OC2 on compare match, clear OC2 at TOP

Compare Output Mode, Phase Correct PWM Mode		
COM21	**COM20**	**Description**
0	0	Normal port operation, OC2 disconnected.
0	1	Reserved

Compare Output Mode, Phase Correct PWM Mode		
COM21	**COM20**	**Description**
1	0	Clear OC2 on compare match when up-counting. Set OC2 on compare match when downcounting.
1	1	Set OC2 on compare match when up-counting. Clear OC2 on compare match when downcounting.

- CS22:0 - Clock Select

CS22	CS21	CS20	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	clk/(No prescaling)
0	1	0	clk/8 (From prescaler)
0	1	1	clk/32 (From prescaler)
1	0	0	clk/64 (From prescaler)
1	0	1	clk/128 (From prescaler)
1	1	0	clk/256 (From prescaler)
1	1	1	clk/1024 (From prescaler)

Timer/Counter Register – TCNT2

Bit	7	6	5	4	3	2	1	0	
	TCNT2[7:0]								TCNT2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Output Compare Register – OCR2

Bit	7	6	5	4	3	2	1	0	
	OCR2[7:0]								OCR2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Asynchronous Status Register – ASSR

Bit	7	6	5	4	3	2	1	0	
	-	-	-	-	AS2	TCN2UB	OCR2UB	TCR2UB	ASSR
Read/Write	R	R	R	R	R/W	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- AS2 - Asynchronous Timer/Counter2
  - 0 : Timer/Counter 2 is clocked from the I/O clock, clkI/O.
  - 1 : Timer/Counter2 is clocked from a Crystal Oscillator connected to the Timer Oscillator 1 (TOSC1) pin.
  - When the value of AS2 is changed, the contents of TCNT2, OCR2, and TCCR2 might be corrupted.

- TCN2UB - Timer/Counter2 Update Busy
  When Timer/Counter2 operates asynchronously and TCNT2 is written, this bit becomes set. When TCNT2 has been updated from the temporary storage register, this bit is cleared by hardware. A logical zero in this bit indicates that TCNT2 is ready to be updated with a new value.

- OCR2UB - Output Compare Register2 Update Busy
  When Timer/Counter2 operates asynchronously and OCR2 is written, this bit becomes set. When OCR2 has been updated from the temporary storage register, this bit is cleared by hardware. A logical zero in this bit indicates that OCR2 is ready to be updated with a new value.

- TCR2UB - Timer/Counter Control Register2 Update Busy
  When Timer/Counter2 operates asynchronously and TCCR2 is written, this bit becomes set. When TCCR2 has been updated from the temporary storage register, this bit is cleared by hardware. A logical zero in this bit indicates that TCCR2 is ready to be updated with a new value.

Timer/Counter Interrupt Mask Register - TIMSK

Bit	7	6	5	4	3	2	1	0	
	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- OCIE2 - Timer/Counter2 Output Compare Match Interrupt Enable
  0 : disable
  1 : enable

- TOIE2 - Timer/Counter2 Overflow Interrupt Enable
  0 : disable
  1 : enable

Timer/Counter Interrupt Flag Register - TIFR

Bit	7	6	5	4	3	2	1	0	
	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	TIFR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- OCF2 - Output Compare Flag 2
  Set (one) when a compare match occurs between the Timer/Counter2 and the data in OCR2. OCF2 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, OCF2 is cleared by writing a logic one to the flag.

- TOV2 - Timer/Counter2 Overflow Flag
  Set (one) when an overflow occurs in Timer/Counter2. TOV2 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV2 is cleared by writing a logic one to the flag.

Special Function I/O Register - SFIOR

Bit	7	6	5	4	3	2	1	0	
	ADTS2	ADTS1	ADTS0	-	ACME	PUD	PSR2	PSR10	SFIOR
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- PRS2 - Prescaler Reset Timer/Counter2

  When this bit is written to one, the Timer/Counter2 prescaler will be reset. The bit will be cleared by hardware after the operation is performed. Writing a zero to this bit will have no effect.

7.13 Serial Peripheral Interface - SPI

SPI Control Register – SPCR

Bit	7	6	5	4	3	2	1	0	
	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- SPIE - SPI Interrupt Enable
  0 : disable
  1 : enable

- SPE - SPI Enable
  0 : disable
  1 : enable

- DORD - Data Order
  0 : MSB of the data word is transmitted first
  1 : LSB of the data word is transmitted first.

- MSTR - Master/Slave Select
  0 : Slave SPI mode
  1 : Master SPI mode

- CPOL - Clock Polarity
  0 : SCK low when idle
  1 : SCK high when idle

CPOL	Leading Edge	Trailing Edge
0	Rising	Falling
1	Falling	Rising

- CPHA: Clock Phase
  The settings of the Clock Phase bit (CPHA) determine if data is sampled on the leading (first) or trailing (last) edge of SCK.

CPHA	Leading Edge	Trailing Edge
0	Sample	Setup
1	Setup	Sample

- SPR1, SPR0 - SPI Clock Rate Select 1 and 0

SPI2X	SPR1	SPR0	SCKFrequency
0	0	0	fosc/4
0	0	1	fosc/16
0	1	0	fosc/64
0	1	1	fosc/128
1	0	0	fosc/2

SPI2X	SPR1	SPR0	SCKFrequency
1	0	1	fosc/8
1	1	0	fosc/32
1	1	1	fosc/64

SPI Status Register – SPSR

Bit	7	6	5	4	3	2	1	0	
	SPIF	WCOL	-	-	-	-	-	SPI2X	SPSR
Read/Write	R	R	R	R	R	R	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- SPIF- SPI Interrupt Flag

  When a serial transfer is complete, the SPIF Flag is set. An interrupt is generated if SPIE in SPCR is set and global interrupts are enabled. If SS is an input and is driven low when the SPI is in Master mode, this will also set the SPIF Flag. SPIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the SPIF bit is cleared by first reading the SPI Status Register with SPIF set, then accessing the SPI Data Register (SPDR).

- WCOL- Write Collision Flag

  The WCOL bit is set if the SPI Data Register (SPDR) is written during a data transfer. The WCOL bit (and the SPIF bit) are cleared by first reading the SPI Status Register with WCOL set, and then accessing the SPI Data Register.

- SPI2X: Double SPI Speed Bit

  When this bit is written logic one the SPI speed (SCK Frequency) will be doubled when the SPI is in Master mode. When the SPI is configured as Slave, the SPI is only guaranteed to work at fosc/4 or lower.

SPI Data Register – SPDR

Bit	7	6	5	4	3	2	1	0	
	MSB							LSB	SPDR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	x	x	x	x	x	x	x	x	

The SPI Data Register is a read/write register used for data transfer between the Register File and the SPI Shift Register. Writing to the register initiates data transmission. Reading the register causes the Shift Register Receive buffer to be read.

7.14 USART

USART I/O Data Register – UDR

Bit	15	14	13	12	11	10	9	8	
	RXB[7:0]								UDR(Read)
	TXB[7:0]								UDR(Write)
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	W	W	W	W	W	W	W	W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

For 5-, 6-, or 7-bit characters the upper unused bits will be ignored by the Transmitter and set to zero by the Receiver.

USART Control and Status Register A – UCSRA

Bit	7	6	5	4	3	2	1	0	
	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	UCSRA
Read/Write	R	R/W	R	R	R	R	R/W	R/W	
Initial Value	0	0	1	0	0	0	0	0	

- RXC - USART Receive Complete
  0 : receive buffer empty
  1 : receive buffer contains unread data

- TXC - USART Transmit Complete
  This flag bit is set when the entire frame in the transmit Shift Register has been shifted out and there are no new data currently present in the transmit buffer (UDR). The TXC-Flag bit is automatically cleared when a transmit complete interrupt is executed, or it can be cleared by writing a one to its bit location.

- UDRE - USART Data Register Empty
  0 : transmit buffer not empty
  1 : transmit buffer empty

- FE - Frame Error
  0 : no frame error
  1 : frame error
  This bit is valid until the receive buffer (UDR) is read. The FE bit is zero when the stop bit of received data is one. Always set this bit to zero when writing to UCSRA.

- DOR - Data OverRun
  This bit is set if a Data OverRun condition is detected. This bit is valid until the receive buffer (UDR) is read. Always set this bit to zero when writing to UCSRA.

- PE - Parity Error
  This bit is set if the next character in the receive buffer had a Parity Error when received and the parity checking was enabled at that point (UPM1 = 1). This bit is valid until the receive buffer (UDR) is read. Always set this bit to zero when writing to UCSRA.

- U2X - Double the USART Transmission Speed

  This bit only has effect for the asynchronous operation. Write this bit to zero when using synchronous operation. Writing this bit to one will reduce the divisor of the baud rate divider from 16 to 8 effectively doubling the transfer rate for asynchronous communication.

- MPCM - Multi-processor Communication Mode

  This bit enables the Multi-processor Communication mode. When the MPCM bit is written to one, all the incoming frames received by the USART receiver that do not contain address information will be ignored. The transmitter is unaffected by the MPCM setting.

USART Control and Status Register B – UCSRB

Bit	7	6	5	4	3	2	1	0	
	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	UCSRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- RXCIE - RX Complete Interrupt Enable

- TXCIE - TX Complete Interrupt Enable

- UDRIE - USART Data Register Empty Interrupt Enable

- RXEN - Receiver Enable

- TXEN - Transmitter Enable

- UCSZ2 - Character Size

  The UCSZ2 bit combined with the UCSZ1:0 bit in UCSRC sets the number of data bits in a frame the receiver and transmitter use.

- RXB8 - Receive Data Bit 8

  RXB8 is the ninth data bit of the received character when operating with serial frames with nine data bits. Must be read before reading the low bits from UDR.

- TXB8 - Transmit Data Bit 8

  TXB8 is the ninth data bit in the character to be transmitted when operating with serial frames with nine data bits. Must be written before writing the low bits to UDR.

USART Control and Status Register C – UCSRC

Bit	7	6	5	4	3	2	1	0	
	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	UCSRC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- URSEL - Register Select

  This bit selects between accessing the UCSRC or the UBRRH Register. It is read as one when reading UCSRC. The URSEL must be one when writing the UCSRC.

- UMSEL - USART Mode Select
  0 : Asynchronous Operation
  1 : Synchronous Operation

- UPM1:0 - Parity Mode

UPM1	UPM0	Parity Mode
0	0	Disabled
0	1	Reserved
1	0	Enabled, Even Parity
1	1	Enabled, Odd Parity

- USBS - Stop Bit Select
  0 : 1 Stop bit
  1 : 2 Stop bits

- UCSZ1:0 - Character Size

UCSZ2	UCSZ1	UCSZ0	Character Size (Frame Size)
0	0	0	5-bit
0	0	1	6-bit
0	1	0	7-bit
0	1	1	8-bit
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	9-bit

- UCPOL - Clock Polarity
  This bit is used for Synchronous mode only. The UCPOL bit sets the relationship between data output change and data input sample, and the synchronous clock (XCK).

UCPOL	Transmitted Data Changed (Output of TxD Pin)	Received Data Sampled (Input on RxD Pin)
0	Rising XCK Edge	Falling XCK Edge
1	Falling XCK Edge	Rising XCK Edge

USART Baud Rate Registers – UBRRL and UBRRH

Bit	15	14	13	12	11	10	9	8	
	URSEL	-	-	-	UBRR[11:8]				UDR(Read)
	UBRR[7:0]								UDR(Write)
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R	R	R	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

The UBRRH Register shares the same I/O location as the UCSRC Register.

- URSEL - Register Select

  This bit selects between accessing the UBRRH or the UCSRC Register. It is read as zero when reading UBRRH. The URSEL must be zero when writing the UBRRH.

- UBRR11:0 - USART Baud Rate Register

Baud Rate (bps)	**fosc = 14.7456 MHz**			
	U2X = 0		U2X = 1	
	UBRR	Error	UBRR	Error
2400	383	0.0%	767	0.0%
4800	191	0.0%	383	0.0%
9600	95	0.0%	191	0.0%
14.4k	63	0.0%	127	0.0%
19.2k	47	0.0%	95	0.0%
28.8k	31	0.0%	63	0.0%
38.4k	23	0.0%	47	0.0%
57.6k	15	0.0%	31	0.0%
76.8k	11	0.0%	23	0.0%
115.2k	7	0.0%	15	0.0%
230.4k	3	0.0%	7	0.0%
250k	3	-7.8%	6	5.3%
0.5M	1	-7.8%	3	-7.8%
1M	0	-7.8%	1	-7.8%
Max	921.6 kbps		1.8432 Mbps	

7.15 Two-wire Serial Interface

TWI Bit Rate Register – TWBR

Bit	7	6	5	4	3	2	1	0	
	TWBR7	TWBR6	TWBR5	TWBR4	TWBR3	TWBR2	TWBR1	TWBR0	TWBR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- TWBR7:0 - TWI Bit Rate Register

$$SCLfrequency = \frac{CPUClockfrequency}{16 + 2(TWBR) \cdot 4^{TWPS}}$$

TWI Control Register – TWCR

Bit	7	6	5	4	3	2	1	0	
	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE	TWCR
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- TWINT - TWI Interrupt Flag

  This bit is set by hardware when the TWI has finished and expects application software response. If the I-bit in SREG and TWIE in TWCR are set, the MCU will jump to the TWI Interrupt Vector. While the TWINT Flag is set, the SCL low period is stretched. The TWINT Flag must be cleared by software by writing a logic one to it. Note that this flag is not automatically cleared by hardware when executing the interrupt routine. Also note that clearing this flag starts the operation of the TWI, so all accesses to the TWI Address Register (TWAR), TWI Status Register (TWSR), and TWI Data Register (TWDR) must be complete before clearing this flag.

- TWEA - TWI Enable Acknowledge Bit

  The TWEA bit controls the generation of the acknowledge pulse. If the TWEA bit is written to one, the ACK pulse is generated on the TWI bus if the following conditions are met:

  1 : The device's own slave address has been received.

  2 : A call has been received, while the TWGCE bit in the TWAR is set.

  3 : A data byte has been received in Master Receiver or Slave Receiver mode. By writing the TWEA bit to zero, the device can be virtually disconnected from the Two-wire Serial Bus temporarily. Address recognition can then be resumed by writing the TWEA bit to one again.

- TWSTA -TWI START Condition Bit

  The application writes the TWSTA bit to one when it desires to become a master on the Two-wire Serial Bus. The TWI hardware checks if the bus is available, and generates a START condition on the bus if it is free. However, if the bus is not free, the TWI waits until a STOP condition is detected, and then generates a new START condition to claim the bus Master status. TWSTA must be cleared by software when the START condition has been transmitted.

- TWSTO - TWI STOP Condition Bit

  Writing the TWSTO bit to one in Master mode will generate a STOP condition on the Two-wire Serial Bus. When the STOP condition is executed on the bus, the TWSTO bit is cleared automatically. In slave mode, setting the TWSTO bit can be used to recover from an error condition. This will not generate a STOP condition, but the TWI returns to a well-defined unaddressed slave mode and releases the SCL and SDA lines to a high impedance state.

- TWWC - TWI Write Collision Flag

  The TWWC bit is set when attempting to write to the TWI Data Register – TWDR when TWINT is low. This flag is cleared by writing the TWDR Register when TWINT is high.

- TWEN - TWI Enable Bit

  The TWEN bit enables TWI operation and activates the TWI interface. When TWEN is written to one, the TWI takes control over the I/O pins connected to the SCL and SDA pins, enabling the slew-rate limiters and spike filters. If this bit is written to zero, the TWI is switched off and all TWI transmissions are terminated, regardless of any ongoing operation.

- TWIE - TWI Interrupt Enable

  When this bit is written to one, and the I-bit in SREG is set, the TWI interrupt request will be activated for as long as the TWINT Flag is high.

TWI Status Register – TWSR

Bit	7	6	5	4	3	2	1	0	
	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0	TWSR
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	1	1	1	1	1	0	0	0	

- TWS7:3 - TWI Status

  These fbits reflect the status of the TWI logic and the Two-wire Serial Bus.

- TWPS1:0 - TWI Prescaler Bits

TWPS1	TWPS0	PrescalerValue
0	0	1
0	1	4
1	0	16
1	1	64

TWI Data Register – TWDR

Bit	7	6	5	4	3	2	1	0	
	TWD7	TWD6	TWD5	TWD4	TWD3	TWD2	TWD1	TWD0	TWDR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	1	

In Transmit mode, TWDR contains the next byte to be transmitted. In Receive mode, the TWDR contains the last byte received.

TWI (Slave) Address Register – TWAR

Bit	7	6	5	4	3	2	1	0	
	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	TWAR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	1	

- TWA6:0 - TWI (Slave) Address Register

- TWGCE: TWI General Call Recognition Enable Bit
  0 : disable General Call recognition
  1 : enable General Call recognition

7.16 Analog Comparator

Analog Comparator Control and Status Register – ACSR

Bit	7	6	5	4	3	2	1	0	
	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	ACSR
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	N/A	0	0	0	0	0	

- ACD - Analog Comparator Disable

  When this bit is written logic one, the power to the Analog Comparator is switched off. When changing the ACD bit, the Analog Comparator Interrupt must be disabled by clearing the ACIE bit in ACSR. Otherwise an interrupt can occur when the bit is changed.

- ACBG - Analog Comparator Bandgap Select

  When this bit is set, a fixed bandgap reference voltage replaces the positive input to the Analog Comparator. When this bit is cleared, AIN0 is applied to the positive input of the Analog Comparator.

- ACO - Analog Comparator Output

  The output of the Analog Comparator is synchronized and then directly connected to ACO. The synchronization introduces a delay of 1 - 2 clock cycles.

- ACI - Analog Comparator Interrupt Flag

  This bit is set by hardware when a comparator output event triggers the interrupt mode defined by ACIS1 and ACIS0. The Analog Comparator Interrupt routine is executed if the ACIE bit is set and the I-bit in SREG is set. ACI is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ACI is cleared by writing a logic one to the flag.

- ACIE - Analog Comparator Interrupt Enable

  When the ACIE bit is written logic one and the I-bit in the Status Register is set, the Analog Comparator Interrupt is activated. When written logic zero, the interrupt is disabled.

- ACIC - Analog Comparator Input Capture Enable

  When written logic one, this bit enables the Input Capture function in Timer/Counter1 to be triggered by the Analog Comparator. The comparator output is in this case directly connected to the Input Capture front-end logic, making the comparator utilize the noise canceler and edge select features of the Timer/Counter1 Input Capture interrupt.

- ACIS1, ACIS0 - Analog Comparator Interrupt Mode Select

ACIS1	ACIS0	Interrupt Mode
0	0	Comparator Interrupt on Output Toggle
0	1	Reserved
1	0	Comparator Interrupt on Falling Output Edge
1	1	Comparator Interrupt on Rising Output Edge

7.17 Analog to Digital Converter

ADC Multiplexer Selection Register – ADMUX

Bit	7	6	5	4	3	2	1	0	
	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	ADMUX
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- REFS1:0 - Reference Selection Bits

REFS1	REFS0	Voltage Reference Selection
0	0	AREF, Internal Vref turned off
0	1	AVCC with external capacitor at AREF pin
1	0	Reserved
1	1	Internal 2.56V Voltage Reference with external capacitor at AREF pin

- ADLAR - ADC Left Adjust Result
  0 : Right adjusted
  1 : Left adjusted
  Changing the ADLAR bit will affect the ADC Data Register immediately

- MUX4:0 - Analog Channel and Gain Selection Bits

MUX 4...0	Single Ended Input	Positive Differential Input	Negative Differential Input	Gain
00000	ADC0	N/A		
00001	ADC1			
00010	ADC2			
00011	ADC3			
00100	ADC4			
00101	ADC5			
00110	ADC6			
00111	ADC7			

MUX 4...0	Single Ended Input	Positive Differential Input	Negative Differential Input	Gain
01000	N/A	ADC0	ADC0	10x
01001		ADC1	ADC0	10x
01010		ADC0	ADC0	200x
01011		ADC1	ADC0	200x
01100		ADC2	ADC2	10x
01101		ADC3	ADC2	10x
01110		ADC2	ADC2	200x
01111		ADC3	ADC2	200x
10000		ADC0	ADC1	1x
10001		ADC1	ADC1	1x
10010		ADC2	ADC1	1x
10011		ADC3	ADC1	1x
10100		ADC4	ADC1	1x
10101		ADC5	ADC1	1x
10110		ADC6	ADC1	1x
10111		ADC7	ADC1	1x
11000		ADC0	ADC2	1x
11001		ADC1	ADC2	1x
11010		ADC2	ADC2	1x
11011		ADC3	ADC2	1x
11100		ADC4	ADC2	1x
11101		ADC5	ADC2	1x
11110	1.22V (VBG)	N/A		
11111	0V (GND)			

MUX = 01010, 01011, 01110, and 01111 not tested for PDIP devices

ADC Control and Status Register A – ADCSRA

Bit	7	6	5	4	3	2	1	0	
	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- ADEN - ADC Enable
  0 : disable
  1 : enable

- ADSC - ADC Start Conversion
  In Single Conversion mode, write this bit to one to start each conversion. In Free Running Mode, write this bit to one to start the first conversion. ADSC will read as one as long as a conversion is in progress. When the conversion is complete, it returns to zero. Writing zero to this bit has no effect.

- ADATE - ADC Auto Trigger Enable

When this bit is written to one, Auto Triggering of the ADC is enabled. The ADC will start a conversion on a positive edge of the selected trigger signal. The trigger source is selected by setting the ADC Trigger Select bits, ADTS in SFIOR.

- ADIF - ADC Interrupt Flag

  This bit is set when an ADC conversion completes and the Data Registers are updated. ADIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ADIF is cleared by writing a logical one to the flag. Beware that if doing a Read-Modify-Write on ADCSRA, a pending interrupt can be disabled. This also applies if the SBI and CBI instructions are used.

- ADIE - ADC Interrupt Enable

  0 : disable
  1 : enable

- ADPS2:0 - ADC Prescaler Select Bits

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC Data Register – ADCL and ADCH

ADLAR = 0

Bit	15	14	13	12	11	10	9	8	
	-	-	-	-	-	-	ADC9	ADC8	ADCH
	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

ADLAR = 1

Bit	15	14	13	12	11	10	9	8	
	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADCH
	ADC1	ADC0	-	-	-	-	-	-	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

When an ADC conversion is complete, the result is found in these two registers. If differential channels are used, the result is presented in two's complement form. When ADCL is read, the ADC Data Register is not updated until ADCH is read. Consequently, if the result is left adjusted and no more than 8-bit precision is required, it is sufficient to read ADCH. Otherwise, ADCL must be read first, then ADCH.

Special Function I/O Register - SFIOR

Bit	7	6	5	4	3	2	1	0	
	ADTS2	ADTS1	ADTS0	-	ACME	PUD	PSR2	PSR10	SFIOR
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- ADTS2...0 - ADC Auto Trigger Source

ADTS2	ADTS1	ADTS0	Trigger Source
0	0	0	Free running mode
0	0	1	Ananlog Comparator
0	1	0	External Interrupt Request 0
0	1	1	Timer/Counter0 Compare Match
1	0	0	Timer/Counter0 Overflow
1	0	1	Timer/Counter Compare Match B

ADTS2	ADTS1	ADTS0	Trigger Source
1	1	0	Timer/Counter1 Overflow
1	1	0	Timer/Counter1 Capture Event

7.18 Boot Loader Support – Read-While-Write Self-Programming

Store Program Memory Control Register – SPMCR

Bit	7	6	5	4	3	2	1	0	
	SPMIE	RWWSB	-	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	SPMCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- SPMIE - SPM Interrupt Enable

  When the SPMIE bit is written to one, and the I-bit in the Status Register is set (one), the SPM ready interrupt will be enabled. The SPM ready Interrupt will be executed as long as the SPMEN bit in the SPMCR Register is cleared.

- RWWSB - Read-While-Write Section Busy

  When a self-programming (Page Erase or Page Write) operation to the RWW section is initiated, the RWWSB will be set (one) by hardware. When the RWWSB bit is set, the RWW section cannot be accessed. The RWWSB bit will be cleared if the RWWSRE bit is written to one after a Self-Programming operation is completed. Alternatively the RWWSB bit will automatically be cleared if a page load operation is initiated.

- RWWSRE - Read-While-Write Section Read Enable

  When programming (Page Erase or Page Write) to the RWW section, the RWW section is blocked for reading (the RWWSB will be set by hardware). To re-enable the RWW section, the user software must wait until the programming is completed (SPMEN will be cleared). Then, if the RWWSRE bit is written to one at the same time as SPMEN, the next SPM instruction within four clock cycles re-enables the RWW section. The RWW section cannot be re-enabled while the Flash is busy with a page erase or a page write (SPMEN is set). If the RWWSRE bit is written while the Flash is being loaded, the Flash load operation will abort and the data loaded will be lost.

- BLBSET - Boot Lock Bit Set

  If this bit is written to one at the same time as SPMEN, the next SPM instruction within four clock cycles sets Boot Lock bits, according to the data in R0. The BLBSET bit will automatically be cleared upon completion of the Lock bit set, or if no SPM instruction is executed within four clock cycles. An LPM instruction within three cycles after BLBSET and SPMEN are set in the SPMCR Register, will read either the Lock bits or the Fuse bits (depending on Z0 in the Zpointer) into the destination register.

- PGWRT - Page Write

  If this bit is written to one at the same time as SPMEN, the next SPM instruction within four clock cycles executes Page Write, with the data stored in the temporary buffer. The page address is taken from the high part of the Z-pointer. The data in R1 and R0 are ignored. The PGWRT bit will auto-clear upon completion of a page write, or if no SPM instruction is executed within four clock cycles. The CPU is halted during the entire page write operation if the NRWW section is addressed.

- PGERS - Page Erase

  If this bit is written to one at the same time as SPMEN, the next SPM instruction within four clock cycles executes Page Erase. The page address is taken from the high part of the Z-pointer. The data in R1 and R0 are ignored. The PGERS bit will auto-clear upon

completion of a page erase, or if no SPM instruction is executed within four clock cycles. The CPU is halted during the entire page write operation if the NRWW section is addressed.

• SPMEN - Store Program Memory Enable

This bit enables the SPM instruction for the next four clock cycles. If written to one together with either RWWSRE, BLBSET, PGWRT' or PGERS, the following SPM instruction will have a special meaning, see description above. If only SPMEN is written, the following SPM instruction will store the value in R1:R0 in the temporary page buffer addressed by the Z-pointer. The LSB of the Z-pointer is ignored. The SPMEN bit will auto-clear upon completion of an SPM instruction, or if no SPM instruction is executed within four clock cycles. During page erase and page write, the SPMEN bit remains high until the operation is completed. Writing any other combination than “10001”, “01001”, “00101”, “00011” or “00001” in the lower five bits will have no effect.

8 Hexadecimal to ASCII Conversion

Bits	Bits 3...0															
7..4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NUL	SOH	STX	ETX	EOT	ENQ	ACK	BEL	BS	HT	LF	VT	FF	CR	SO	SI
1	DLE	DC1	DC2	DC3	DC4	NAK	SYN	ETB	CAN	EM	SUB	ESC	FS	GS	RS	US
2	SP	!	"	#	$	%	&	’	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
6	‘	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	DEL

9 PIN Assignments